Q2.

**On the IAS, describe the process that the CPU must undertake to read a value from memory and to write a value to memory in terms of what is put into the MAR, MBR, address bus, data bus, and control bus.**

**Solution:-**

To read a value from memory, the CPU puts the address of the value it wants into the MAR. The CPU then asserts the Read control line to memory and places the address on the address bus. Memory places the contents of the memory location passed on the data bus. This data is then transferred to the MBR. To write a value to memory, the CPU puts the address of the value it wants to write into the MAR. The CPU also places the data it wants to write into the MBR. The CPU then asserts the Write control line to memory and places the address on the address bus and

the data on the data bus. Memory transfers the data on the data bus into the

corresponding memory location.

**Q3.**

Consider two different machines, with two different instruction sets, both of which have a clock rate of 200 MHz. The following measurements are recorded on the two machines running a given set of benchmark programs:

Solution:-



a. Determine the effective CPI, MIPS rate, and execution time for each machine.

b. Comment on the results.

b. Even though, machine B has a higher MIPS than machine A, it needs a longer CPU time to execute the similar set of benchmark programs (instructions

**Q.4**

**A benchmark program is run on a 40 MHz processor.The executed program consists of 100,000 instruction executions, with the following instruction mix and clock cycle count:**



Determine the effective CPI, MIPS rate, and execution time for this program.

Solution:-

CPI is the average Clocks per instructions =

45000 + (2\*32000) + (2\*15000) + (8000\*2) / (100 000) = 155 / 100 = 1.55

MIPS =40 M clocks / sec \* (1/1.55 clocks per instruction) = 40 / 1.55 / 1000000 = 25.8 MIPs

Execution time = (100 000 instructions) \* 1.55 CPI = 155 000 cyles \* 1/40M sec = 0.003875 = 3.87 ms

Stallings: CPI = 1.55; MIPS rate = 25.8; Execution time = 3.87 ns.

**Q.5**

**Consider two SRC programs having three types of instructions given as follows**

|  |  |  |
| --- | --- | --- |
| Number of .. | Program 1 | Program 2 |
| data transfer instructions | 2 | 1 |
| control instructions | 2 | 5 |
| ALSU Instructions | 2 | 1 |

|  |  |
| --- | --- |
| Instruction Type | CPI |
| Control | 2 |
| ALSU | 3 |
| Data Transfer | 4 |

Compare both the programs for the following parameters

1. Instruction count
2. Speed of execution

Solution:

1. Instruction count IC.

IC for program 1= 2+2+2=6

IC for program 2= 1+5+1=7

1. For execution time we can use the following SRC specifications.

ET = IC x CPI x T

ET1= (2x2)+(2x3)+(2x4)

= 18

ET2 =(5x2)+(1x3)+(1x4)

=17

Note: Since both programs are executing on the same machine, the T factor can be ignored while calculating ET.

**Q.6**

**Consider a machine having a 100 MHz clock and three instruction types with following**

**parameters.Now suppose that two different compilers generate code for the same program.**

**The instruction count for each is given as follows**

|  |  |
| --- | --- |
| Instruction Type | CPI |
| Control | 2 |
| ALSU | 3 |
| Data Transfer | 4 |

|  |  |
| --- | --- |
| Instruction Type | CPI |
| Control | 2 |
| ALSU | 3 |
| Data Transfer | 4 |

Solution:

First we find the CPI for both code sequences

Since CPI = clock cycles for each type of instruction / IC

CPI1= (5x2 + 1x3 + 1x4)/ 7 = 2.43

CPI2= (10x2 +1x3 + 1x4)/12 = 2.25

As MIPS= Clock Rate/ (CPI x 106 )

MIPS1= 100 x 106 / (2.43 x 106)

= 41.15

MIPS2=100 x 106 / (2.25 x 106)

= 44.44

Hence the code generated by compiler 2 has higher MIPS Rating.